AN2951
Application note

3 kW fixed-off-time (FOT) power factor correction

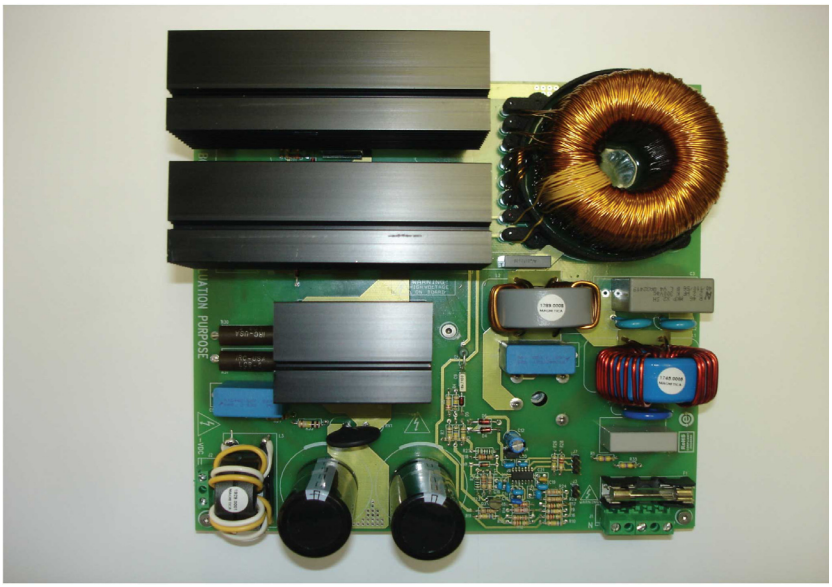
Introduction

In recent years, regulation in terms of electrical efficiency, electromagnetic noise, and reliability of the electronic apparatus, in all the application fields, are pushing to use power factor correction in almost all applications; from low power range to high power range, and from industrial to domestic applications.

For this reason the design of a new PFC architecture is required to satisfy these new priorities. The PFC must work from a few watts to thousands of watts and also use cheap devices and materials. The design described in this paper is able to cover most of the common domestic and industrial applications.

A few examples of the application fields are: air conditioning, inverters (for fans and pumps), welding machinery, and industrial battery chargers.

Figure 1. STEVAL-ISF001V1, 3 kW FOT PFC board-top view



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1 PFC working mode general description

Essentially two methods of controlling power factor corrector (PFC) preregulators are well known and used. Fixed frequency PWM average current control and fixed-on-time variable frequency control.

The first method is a relatively complex control that requires a controller (e.g. L4981) which is usually sophisticated and expensive. With this method the current on the inductor is continuous and oscillates around the sinusoidal semiperiod value with a predetermined and fixed ripple.

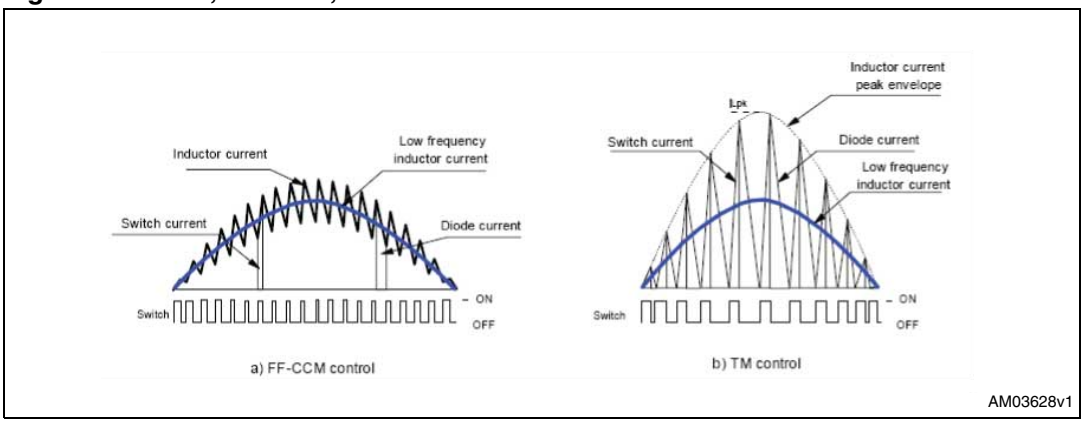
In the second method the current on the inductor is discontinuous, reaching zero and starting to increase again on each switching period. It is cheaper but cannot be used for high power range applications due to the large peak current it causes during its action according to the load.

Other than these two methods, a third may be approached. Instead of maintaining the on-time fixed, such as TM PFC, the Toff is kept constant and the Ton is free to be changed in order to modulate the power drained from the source according to the load. This is called the “fixed-off-time modulation method”. Obviously, it is also a variable frequency control with some advantages, in particular the spread of noise energy conducted on the net that gives a lower noise power density in respect to a fixed frequency modulation, which simplifies the design and realization of the main filter required to match the EMC regulation.

The interesting point is that this kind of modulation can be obtained using a simple and cheap controller designed for TM (transition mode), e.g. the L6562 or L6563 by STMicroelectronics.

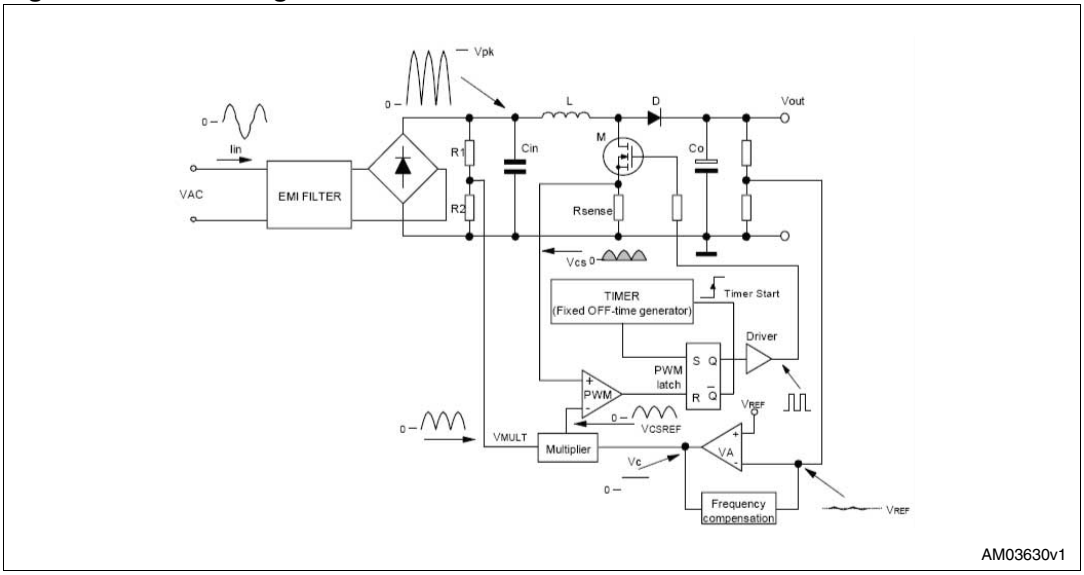
This method, with a complete theoretical explanation, is well described and depicted in the AN1792 application note by STMicroelectronics; “Design of fixed-off-time controller PFC preregulators with L6562”. We suggest first reading the antecedent AN1792 application note before continuing to read. Starting from this point we refer to the AN1792 to study in depth the design of a 3 kW FOT PFC preregulator.

Figure 2. Line, inductor, switch and diode current on TM and CCM control



2 Practical implementation of an FOT-controlled PFC preregulator

Figure 3. Block diagram of a fixed-off-time architecture



The power conversion topology is classically based on a boost converter modulated to drain a current that follows the shape of the main AC voltage; in order to have a current as sinusoidal as possible, and in phase with the mains, assuring a high power factor and low THD (total harmonic distortion).

The architecture is based on a fixed-off-time generator, a multiplier, a PWM generator, and a voltage amplifier with frequency compensation to implement the output voltage control against the load variations.

To modulate the current on the inductor a current reading is required. The information regarding the peak current can be retrieved by reading, at the end of the Ton period, the voltage drop on a sense resistor in series with the power switch.

The input at the multiplier (Vmult) is responsible of the “shaping” action dictated by the input AC voltage.

The amplitude of the sinusoidal shaping action that directly imposes the reference to the PWM generator is given by the voltage loop control through the error amplifier and the frequency compensation.

In practice, the PWM block fixes the Ton time. As soon as the current on the power switch reaches the value fixed by the output multiplier level (Vcsref), the output of the comparator resets the flip-flop and turns off the power switch.

At the same time the output of the comparator triggers the timer and the counting of the off-time starts. At the end of the fixed-off-time period the timer block sets the flip-flop and the power switch is again switched on.

These functions can be implemented by using a TM controller such as the L6562 or L6563.

3 Fixed-off-time using the L6562

The circuit to implement FOT control with the TM L6562 driver is shown in *Figure 4*.

On the L6563 driver the V_{ZCD} pin is available which allows, working in TM, to detect the zero crossing of the current on the main inductor. Here we show how it is possible to use this pin to force the driver to work in a fixed-off-time mode.

During Ton of the power switch, pin 7 (GD gate driver) is high and the D diode is direct biased. Under this condition, because the output GD is at Vcc (usually 15v), the voltage on V_{ZCD} is internally clamped to $V_{ZCDclamp}$=5.7 V.

During Toff, the GD pin is low, the D diode is reverse-biased and the C capacity can be discharged by the R resistor following the exponential law:

Equation 1

$$V_{ZCD} = V_{ZCDclamp} e^{\frac{-t}{RC}}$$

Until the voltage on the V_{ZCD} pin reaches the triggering threshold (about 1.4 V) the power switch is switched on. Using this passive net the Toff can be set by design. Solving *Equation 1* in respect to the time the Toff can be calculated:

Equation 2

$$Toff = RC \ln \frac{V_{ZCDclamp}}{V_{ZCDtrigger}} \approx 1.4RC$$

As suggested with AN1792, it is better to select a capacitor first, and calculate the needed resistor to set the desired Toff.

The passive net composed by CS and Rs assures that, as soon as the V_{GD} goes high the C capacitor is charged at $V_{ZCDclamp}$ as quickly as possible without exceeding the current capability of the V_{ZCD} pin.

Equation 3

$$\frac{V_{GD} - V_{ZCDclamp} - V_F}{I_{IZCD} + \frac{V_{ZCDclamp}}{R}} < R_S < R \frac{V_{GD} - V_{ZCDclamp} - V_F}{V_{ZCDclamp}}$$

Cs acts as a speed-up capacitor needed to instantaneously charge C in case of very short Ton when working at high AC input voltage and light load.

The Cs capacitor should be chosen as:

Equation 4

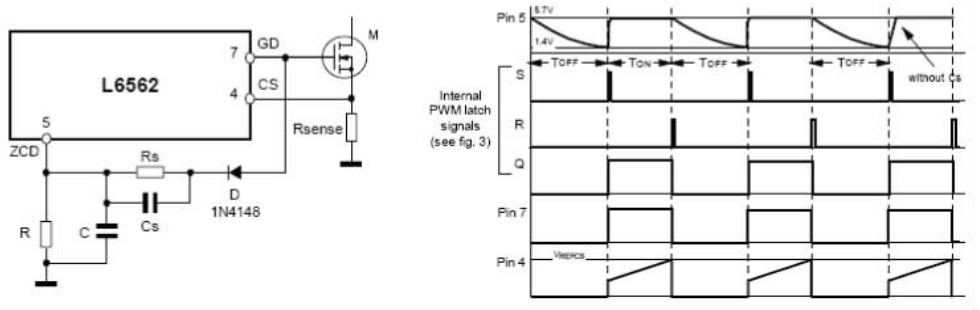
$$C_s < C \frac{V_{ZCDclamp}}{V_{GD} - V_{ZCDclamp} - V_F}$$

The FOT control allows a CCM operation and high power capability but with the circuit complexity and driver performance generally sufficient on a TM controller.

This is possible because a characteristic of an FOT control is the possibility to use a simple peak current control instead of a more difficult average mode control as required on a classic CCM control.

For further details and implications of FOT control, please refer to the AN1792 application note.

Figure 4. FOT control with the L6562 and relevant timing waveforms



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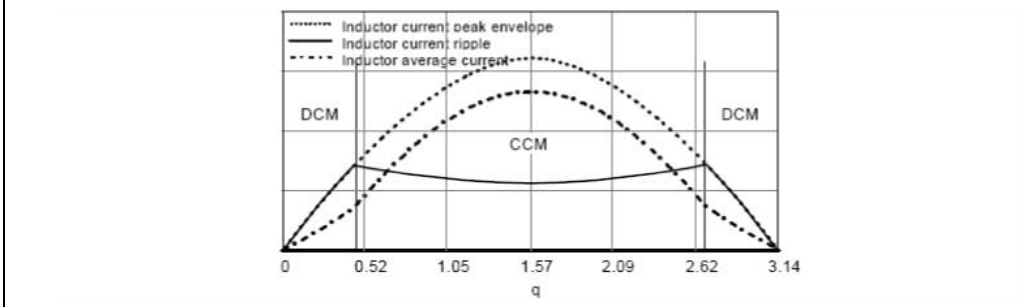
4 Working mode along line period in a FOT PFC

Figure 5. Working mode along line semiperiod



In *Figure 5* a full description of the main characteristics and the evolution of some key parameters of an FOT, along the semiperiod of the input AC source, is shown. The dotted line represents the envelope of the peak inductor current. As clearly noted, the shape is sinusoidal as required, in order to have a high power factor. This is a consequence of the Ton modulation carried out by following the output of the multiplier Vcsref (see *Figure 3*).The dash-dot line represents the inductor average current. A distortion on the average instantaneous boost current value can be noted around the zero crossing of the line voltage. Though this aspect is not negligible, it is inevitable. It is due to the working mode (discontinuous) in this region. A trade off between operating frequency and line current distortion has also to be taken into account. To limit the line current distortion at high line voltage a suitably large Toff must be selected; also fixing a limited current ripple on the boost inductor, a bigger inductor size may be needed. Returning to *Figure 5*, the continuous line represents the inductor current ripple along the sinusoidal semiperiod (0 -π).

Some important considerations can be taken into account regarding this matter. Two kinds of working modes can be recognized during the semiperiod; DCM and CCM. For low input voltage (near zero crossing of the mains) the converter works in discontinuous mode; this means that the current reaches zero for a certain time during the switching period. The behavior along the semiperiod is symmetrical in respect to the centre of the semiperiod (π/2). Two points can be identified where the current ripple on the boost inductor is equal to the peak value. Those two points dictate the transition between the discontinuous and continuous mode, therefore we call the respective angle; the transition angle. If θ is the transition angle:

Equation 5

$$\text{DCM} \quad 0 < t < \frac{\theta}{\omega} \quad \text{and} \quad \frac{\pi - \theta}{\omega} < t < \frac{\pi}{\omega}$$

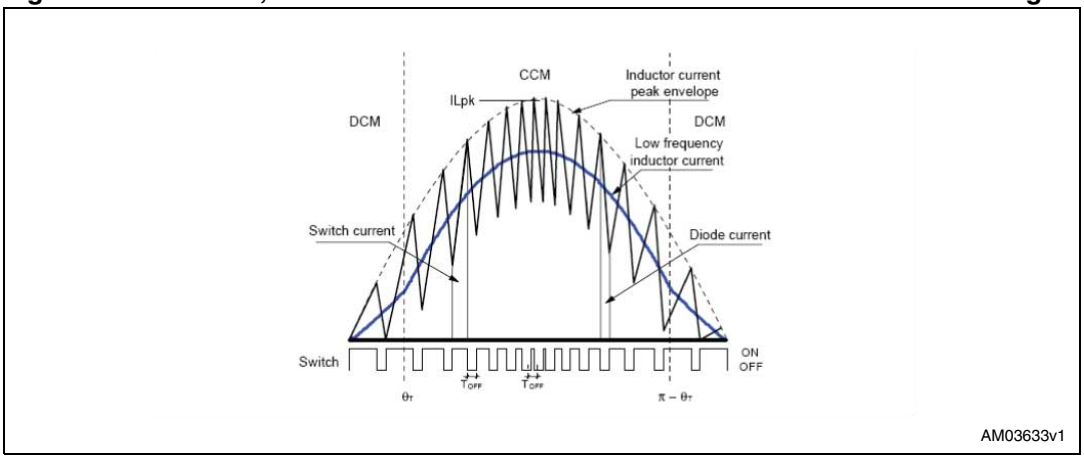
Equation 6

$$\text{CCM} \quad \frac{\theta}{\omega} < t < \frac{\pi - \theta}{\omega}$$

The amplitude of the DCM portion, and so the angle, are not fixed but depends on input voltage and load power. As the power is reduced, the DCM region increases.

For very light load and high input voltage the working mode can be completely discontinuous. The width of the DCM portion depends on the ripple chosen for the boost inductor current during the design calculation. In a Fixed power load, the smaller the ripple imposed during the design, the narrower the DCM portion is. The drawback is that a bigger, and therefore more expensive and cumbersome, inductor is required. A trade off between these parameters needs to be accepted. This parameter is usually fixed as a percentage value of the maximum peak current on the inductor (min Vac max output power) and a value between 0.2 (20%) and 0.4 (40%) is usually adopted. We call this parameter K_r. In the DCM region the stress on the power switch, due to the reverse recovery of the boost diode, is reduced; moreover the switching losses on the power switch due to the turn on under a zero current condition are also reduced. As the DCM portion can also reach 30% of whole semiperiod, this can help to improve the efficiency, thanks to soft switching operation. In *Figure 6* an example of the current on: line, power switches, and diode; on a semiperiod of the input AC voltage, is depicted.

Figure 6. Inductor, switch and diode currents in a CCM FOT-controlled PFC stage



As shown in *Figure 6* the current on the inductor increases during Ton (inductor magnetization) and decreases during Toff. The peak of the inductor current, cycle by cycle, is enveloped by $I_{lpeak} \sin \omega t$. As Toff is fixed by design, only Ton is free to change, the frequency is variable along the semiperiod. In particular, it is at maximum on the peak of the input voltage (where Ton is minimum) and minimum at the transition angle (transition between CCM and DCM and vice versa). The switching frequency is fixed during the entire DCM portion. Some analogous observations may be done on the boost inductor current ripple. It is at a minimum on the top of the sinusoid and maximum at the transition angle. As a consequence of this, a relationship between transition angle and K_r can be provided:

Equation 7

$$K_r = \sin\theta = \frac{I_{Iripple}}{I_{lpk}}$$

Equation 7 comes from the definition of K_r as the ratio between the maximum current ripple amplitude to the inductor peak current. At the transition angle (boundary point CCM-DCM), as the working mode starts to go into DCM, the current ripple is equal to the peak current sinusoidal envelop value multiplied by $\sin\theta$ (remember that θ is the transition angle).

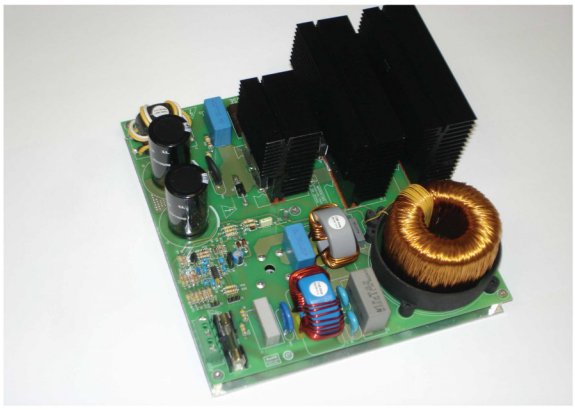
The line current is sinusoidal in the portion between the two transition angles, but it is linear in the two DCM portions. For this reason it is impossible to have a power factor equal to 1 using fixed-off-time.

For further information and for a collection of all the theoretical formulas involved in FOT modulation theory, also including some 3-D plots of various quantity change within one half cycle of the main voltage and load variation, please refer to the AN1792 application note.

5 Practical 3 kW FOT PFC design

Here is a description of the rules and calculations used to design the 3 kW FOT PFC. The prototype board can be ordered with the code STEVAL-ISF001V1.

Figure 7. 3 kW FOT PFC demonstration board (STEVAL-ISF001V1)



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In *Table 1*, the electrical specifications of the STEVAL-ISF001V1 design are shown.

Table 1. Technical specifications

Parameter	Value
Line voltage	185 to 265 Vac
Line frequency	50 Hz
Regulated output voltage	400 Vdc
Maximum output power	3000 W
Vout ripple (%)	5%
Maximum switching frequency	55 kHz
Inductor current ripple (Kr)	0.25

To properly calculate the Toff on a fixed-on-time modulator, we need to consider that it must be of a proper size to assure that at high voltage input and light load, it is enough to avoid distortion on the input current.

To do this, we start by considering the basic relationship, valid on a boost topology working in CCM, between Vout and Vin.

Equation 8

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-\delta}$$ Where: δ is duty cycle

Equation 9

$$\delta = \frac{Ton}{T}$$ Where T is the switching period

Equation 10

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-\frac{Ton}{T}} = \frac{T}{T-Ton} = \frac{T}{Toff} = \frac{1}{f_{sw}Toff} \quad \text{From that:} \quad Toff = \frac{V_{in}}{V_{out}f_{sw}}$$

In order to avoid main current distortion when working at high line voltage the Toff must be selected at greater than a minimum value.

Therefore, if a limit on the maximum switching frequency wants to be respected:

Equation 11

$$Toff > \frac{Vinrms_{min}\sqrt{2}}{Voutfsw_{max}}$$

Where fsw_{max} is the maximum frequency wanted for the switching. (see *Section 3*).

Starting from now we can define two quantities useful for the calculation:

Equation 12

$$K_{max} = \frac{Vinrms_{max}\sqrt{2}}{Vout}$$

Equation 13

$$K_{min} = \frac{Vinrms_{min}\sqrt{2}}{Vout}$$

These two relations represent the Vpk/Vout ratio at minimum and maximum AC main input.

Starting from the same considerations of *Equation 10*, it is possible to calculate the minimum Ton required by the boost:

Equation 14

$$Ton_{min} = \frac{1-K_{max}}{K_{max}}Toff$$

It is simple to verify that:

Equation 15

$$fsw_{max} = \frac{1}{Ton_{min}+Toff}$$

Particular attention must be paid to verify the maximum switching frequency of the system. In fact, the Ton_{min} is calculated according to the maximum input voltage required by the technical specification. In this condition, the reduction of the on-time, due to the greater input voltage and with the off-time fixed, pushes the switching frequency to a higher value. If a maximum switching frequency wants to be respected, a lower value must be posted into the relationship (*Equation 17*).

The full calculation requires a recursive method to verify that, imposing the switching frequency at low voltage input, the switching frequency at high voltage input doesn't overcome the maximum wanted. See *Equation 22* and *Equation 23*.

This could prevent using high frequency switching (at low voltage input) in order to have a small inductor size.

Following the definition of current ripple and parameter (see above), it is possible to calculate ΔI_{ripple}.

Equation 16

$$K_r = \frac{\Delta I_{ripple}}{Ilmain_{peak} + \frac{\Delta I_{ripple}}{2}} \quad \text{Solving by } \Delta I_{ripple}$$

Equation 17

$$\Delta I_{ripple} = \frac{2K_r Ilmain_{peak}}{(2 - K_r)}$$

If we want to impose the maximum current ripple calculated by *Equation 24*, as it is at transition angle, the relation between the ripple and the value of the boost inductor is:

Equation 18

$$L = \frac{Vout - K_r\sqrt{2}Vinrms_{min}}{\Delta I_{ripple}} Toff$$

While remembering that K_r=sinθ; the input voltage at the transition angle is $\sqrt{2}Vinrms_{min}K_r$:

Equation 19

$$K_{min} = \frac{\sqrt{2} * 185}{400} = 0.652$$

Following the information above and the technical specifications summarized in *Table 1*, the calculations of the 3 kW FOT board are:

Equation 20

$$K_{max} = \frac{\sqrt{2} * 265}{400} = 0.934$$

Equation 21

$$Toff > \frac{185 * \sqrt{2}}{400 * 35 * 10^3} = 16.3\ \mu s$$

Equation 22

$$Ton_{min} = \frac{1 - 0.934}{0.934} * 16.3\ \mu s = 1.15\ \mu s;$$

Equation 23

$$fsw_{max} = \frac{1}{1.15\ \mu s + 16.3\ \mu s} \approx 57\ kHz \quad (fsw_{max} @ Vinrms_{max})$$

Equation 24

$$Iin_{rms} = \frac{P_{out}}{\eta Vinrms_{min} PF} = \frac{3000}{0.95 * 185 * 0.99} = 17.24\ A$$

Equation 25

$$\Delta I_{ripple} = \frac{2 * 0.25 * \sqrt{2} * 17.24}{(2 - 0.25)} \approx 6.95 \text{ A}$$

Equation 26

$$L \geq \frac{400 - 0.25 * \sqrt{2} * 185}{6.95} 16.3 * 10^{-6} \approx 785 \ \mu H$$

Choosing for C a value of 1.5 nF the R resistor = 7.6 kΩ. (8.2 kΩ is used with a slightly greater Toff).

For the calculation of the output electrolytic capacitors the following formula may be used. Fixing the maximum voltage ripple to 10% of the output voltage we have:

Equation 27

$$V_{out_ripple_PkPk} \leq V_{out} * 0.1 = 40 \text{ V}$$

$$V_{out_ripple_Pk_Pk} = \frac{I_{out}}{\pi(2f_{mains})C_{out}}$$

$$C_{out} = \frac{I_{out}}{\pi(2f_{mains})V_{out_ripple_Pk_Pk}} = \frac{7.5}{\pi * 2 * 50 * 40} = 597 \ \mu F$$

2 capacitors of 330 µF can be paralleled on the output.

6 Power dissipation

In this section some calculations and theoretical relations are shown.

The calculation of the power dissipation on active devices on the board, under the right working conditions and accepting some approximations, may be considered standard and no different to a PFC working in CCM.

Let's start from the calculation of the current on the output at full load:

Equation 28

$$I_{out} = \frac{P_{out}}{V_{out}} = \frac{3000}{400} = 7.5 \text{ A}$$

As already calculated above the RMS value of the current on the mains is 17.24 A. The peak current is:

Equation 29

$$I_{in_pk} = \sqrt{2} * I_{in_rms} = \sqrt{2} * 17.24 = 24.3 \text{ A}$$

Also the input average current may be calculated as:

Equation 30

$$I_{in_AVG} = \frac{2I_{in_PK}}{\pi} = \frac{2 * 24}{\pi} = 15.28 \text{ A}$$

The total dissipation on the bridge is:

Equation 31

$$P_{bridge} = 2V_F I_{in_AVG} = 2 * 1 * 15.28 \cong 30.5 \text{ W}$$

In order to calculate the power dissipated on the boost diode we need to evaluate the RMS on the diode.

Equation 32

$$I_{Drms} = \frac{P_o}{V_{in_pk(min)}} \sqrt{\frac{16 * V_{in_pk(min)}}{3\pi V_{out}}} = \frac{3000}{261} \sqrt{\frac{16 * 261}{3\pi * 4000}} = 11.5\sqrt{1.1} \cong 12 \text{ A}$$

Equation 33

$$P_{diode} = P_{cond} + P_{sw} = P_{cond} + \frac{1}{2} f_{sw} V_{out} Q_{rr}$$

From the datasheet of the STTH12S06 diodes used as boost diodes we find:

Equation 34

$$V_F(125^{\circ}) = 1.5 \text{ V} \quad Q_{rr} = 160 \text{ nC} \quad t_{rr=14ns}$$

Equation 35

$$P_{diode} = V_F I_F + \frac{1}{2} f_{sw} V_{out} 2Qrr = 1.5 * 12 + 55 \text{ kHz} * 400 * 160 * 10^{-9} = 18 + 3.52 = 21.52 \text{ W}$$

Where we considered doubling the Qrr because two diodes in parallel are used. For the used power switches we have:

Equation 36

$$R_{DS(on)(125°)} = 1.9R_{DS(on)(25°)} = 1.9 * 90\ m\Omega = 0.171\ \Omega$$

Equation 37

$$C_{oss} = 1250_{pF}$$

Equation 38

$$t_r = 30\ \mu s$$

Equation 39

$$I_{DS_{pk}} = I_{L_{pk}} = I_{in_pk} + \frac{I_{ripple}}{2} = 24.3 + \frac{6.95}{2} = 27.78\ A$$

With two power switches in parallel we have 13.89 A for each.

Equation 40

$$I_{DS_{rms}} = \frac{P_{out}}{\eta * PF * V_{inminpk}} \sqrt{2 - \frac{16V_{inminpk}}{3\pi V_{out}}} = \frac{3000}{0.95 * 0.99 * 261} \sqrt{2 - \frac{16 * 261}{3\pi * 400}} = 11.53\ A$$

Equation 41

$$P_{cond} = \frac{1}{2}(I_{Drms})^2 * R_{DS(on)(125°)} = \frac{1}{2} * 11.53^2 * 0.171 = 11.35\ W$$

Equation 42

$$P_{sw} = 2f_{sw}(t_r V_{out} \frac{I_{in_pk}}{2} + 2\frac{1}{2} C_{oss} V_{out}{}^2) =$$

$$= 2 * 55 * 10^3 (30 * 10^{-9} * \frac{27.78}{2} * 400 + 1250 * 10^{-12} * 400^2) = 42\ W$$

Equation 43

$$P_{Tot_mos} = P_{cond} + P_{sw} \cong 53\ W$$

7 Schematic and circuit description

In *Figure 8* the detailed schematic of the board is given.

Starting from the input section a common mode EMC filter is fitted in order to be compliant with the EMC limit rule suited to industrial and domestic application. (EN55014 and EN55022).

The alternative voltage, from the mains, is than rectified by the input low frequency bridge that provides, to the next boost stage, a rectified sinusoidal waveform with a frequency doubled in respect to the input main waveform. The C22 capacitor (0.68uF) is calculated as having a residual ripple around the sinusoidal envelope at maximum load and minimum input voltage of 6% of the Vin peak value.

The main boost inductor, designed and realized by MAGNETICA (Italy), is a ferrite inductor core designed to minimize the hystereses losses.

The technical sheet, with a complete order code, is shown in *Figure 9*.

The inductor has a secondary side winding that provides the low voltage auxiliary supply to the L6563 driver.

At the startup, the current and voltage on the main inductor is still zero, so any voltage can be generated by the secondary auxiliary winding. In this condition, and only during the startup, the R7 and R13 resistors, 150 kΩ each, with the D4 Zener diode (fitted for limitation purposes) charge the C12 capacitor and supply the driver that starts the PWM operation. As soon as the PWM signal starts to switch, a voltage is present across the auxiliary winding, so the low supply voltage across the C12 capacitor is maintained.

The two paralleled boost diodes conduct the peak inductor current at the end of the Ton period. At the maximum power and minimum input voltage the peak current can reach 29 A.

The part number for the diodes is STTH12S06. This diode has a trr of only 14 ns that help to reduce switching losses caused by reverse recovery, relevant in cases of continuous switching operations as in this case.

The D2 diode and the NTC resistor RV1 are used to limit the inrush current, due to the electrolytic capacitor on the output, during the startup.

The chosen switching devices are two power MOSFETs from the MDmesh ^{TM} II family, STW55NM60.

Two Power MOSFETs can be mounted on the board, working in parallel in order to reduce $R_{DS(on)}$ and according to power dissipation. A solution with the new device from the MDmesh^{TM} V family was tested with interesting results in terms of efficiency. Using only one device STW77N65M5 an output power of 2.5 kW may be supplied by the systems.

In order to properly drive the two power MOS and to minimize switching losses, during the on and off transient, a small push-pull driver was interposed between the driver and the two gates. A reading of the current conducted by the two power MOSFETs, equal to the current on the main inductor during the Ton period, is necessary to the driver in order to fix the right current level on the inductor according to the input instantaneous voltage and the output power delivered to the load.

This current is sensed by a sensing resistor implemented paralleling two 0,07 Ω non-inductive sensing resistors. The output DC bus voltage is sensed by the driver through the resistive net composed by R12, R16, R17, and R24.

As stated on the L6563 datasheet this pin is used to sense the PFC preregulator output voltage and is used for protection purposes.

If the voltage at the pin exceeds 2.5 V the IC is shut down, its consumption goes almost to the startup level and this condition is latched. The PWM_LATCH pin is asserted high.

Normal operation can be resumed only by cycling the Vcc. This function is used for protection in case the feedback loop fails.

The feedback loop is otherwise implemented by the net R9, R10, R11, R14, and R15.

The RC net, on the ZCD pin, is used to fix the desired Toff time according to the sizing calculation of the application (refer to the full explanation and practical calculation already given). The small signal BJT Q3 is used to implement a Toff modulation according to the input voltage. At low voltage instant time of the input waveform, (near the zero crossing of the input sinusoidal supply) in order to minimize the distortion on the input current, due to the low voltage in input, the Toff period needs to be reduced. Acting in this way the ratio between the Ton and Toff is increased and the distortion on the input current can be reduced.

The J4 jumper present on the board allows the choosing of two possible solutions of low voltage supply of the driver. Inserting the jumper on the right, the auxiliary supply, produced via the winding on the main inductor, is used; otherwise an external DC power source (20 Vdc 100 mA min) can be connected.

This can be useful during debug of the board or if an inductor without any secondary winding is to be tested.

On the J7 some control signals of the driver chip are available (refer to the L6563 datasheet).

Figure 8. 3 kW PFC STEVAL-ISF001V1 schematic

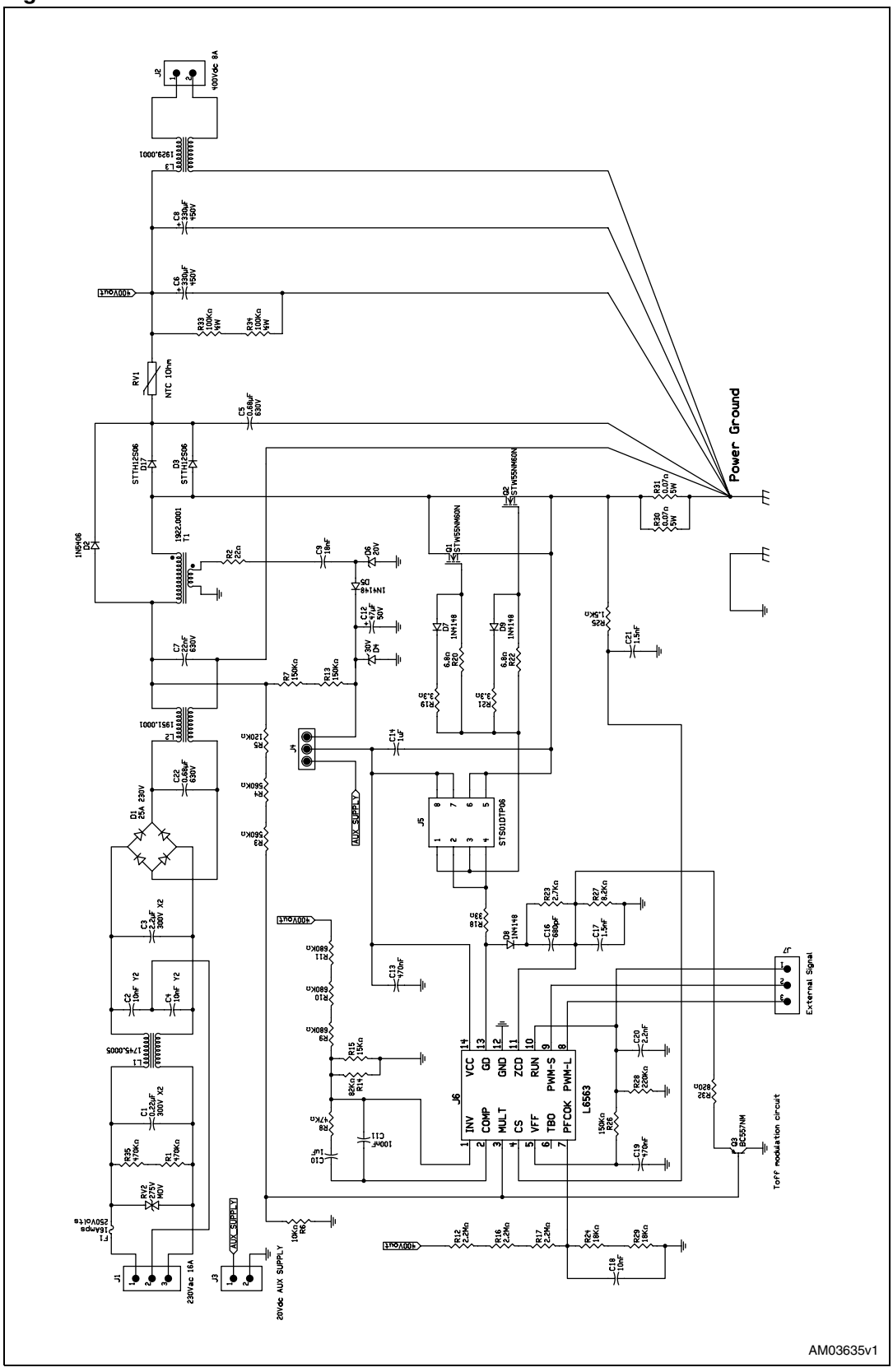


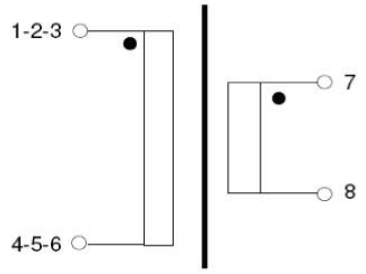
Figure 9. MAGNETICA technical sheet

STP 04	Specifica Tecnica di Prodotto	*Codice* : **1922.0001**
Prodotto: **Induttanza di blocco 1.5mH 13A**		
Cliente: **STMicroelectronics**		*Codice cliente:*

APPLICAZIONE TIPICA

INDUTTORI PER CONVERTITORI DC/DC BUCK, BOOST E BUCK-BOOST, IDEALE ANCHE NELLE APPLICAZIONI HALF-BRIDGE, PUSH-PULL E FULL-BRIDGE

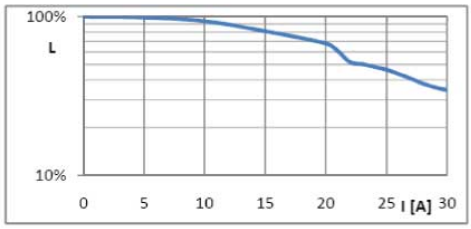
SCHEMA ELETTRICO



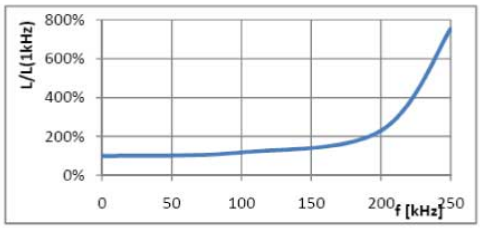
SPECIFICHE TECNICHE

INDUTTANZA *(MISURA 1KHZ, TA 20 °C)*	
TERMINALI 1,2,3-4,5,6	1.5mH ±15%
TERMINALI 7-8	18uH ±15%
RESISTENZA *(MISURA DC, TA 20 °C)*	
TERMINALI 1,2,3-4,5,6	100mΩ MAX
TERMINALI 7-8	185mΩ MAX
TENSIONE DI LAVORO *(F 70KHZ, IR 13A, TA 20 °C)*	500V MAX
CORRENTE DI LAVORO *(MISURA DC , TA 20 °C)*	13A NOM
CORRENTE DI SATURAZIONE *(MISURA DC, L ≥ 35%NOM, TA 20 °C)*	29A MAX
FREQUENZA DI RISONANZA *(TA 20 °C)*	250KHZ NOM
TEMPERATURA OPERATIVA *(IR 13A MAX)*	-10°C÷+45°C
DIMENSIONI	75x80 H62mm
PESO	820g CIRCA

INDUTTANZA IN FUNZIONE DELLA CORRENTE



INDUTTANZA IN FUNZIONE DELLA FREQUENZA



FUNZIONE DEI TERMINALI

TERMINALE (*)	*FUNZIONE*	*TERMINALE(*)*	*FUNZIONE*
1_A	INIZIO AVV. INDUTTANZA PFC	5_B	FINE AVV. INDUTTANZA PFC
2_A	INIZIO AVV. INDUTTANZA PFC	6_B	FINE AVV. INDUTTANZA PFC
3_A	INIZIO AVV. INDUTTANZA PFC	7	INIZIO AVV. AUSILIARIO
4_B	FINE AVV. INDUTTANZA PFC	8	FINE AVV. AUSILIARIO

(*)I TERMINALI CHE HANNO LO STESSO PEDICE VANNO COLLEGATI INSIEME NELLO STAMPATO

MAGNETICA

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8 Experimental results and scope acquisition

A complete set of measurements, changing supply voltage and load condition, have been collected and are shown below.

An electronic dummy load was connected at the output of the board and two electronic watt meters to get a precise measurement of:

- Input AC power
- PF and THD
- Output power
- Output voltage

In addition to this, an oscilloscope was also used to measure the Vout ripple and to obtain some images of significant waveform.

The efficiency was calculated off-line using the collected measurements.

The following three tables (*Table 2*, *Table 3*, and *Table 4*) contain the data for three different values of the input voltage chosen in the nominal range (185<Vac<265).

Table 2. Measurements for Vinac = 185 Vac

Pout	Pin	eff.(%)	PF	THD	Vout	Voutripple	Ripple%
156	163	95.7	0.940	18.3	406	8	2.0
306	319	95.9	0.971	11.5	406	12	3.0
457	474	96.4	0.984	8.5	406	14	3.4
606	628	96.5	0.989	7.1	406	16	3.9
755	782	96.5	0.992	6.4	406	16	3.9
906	938	96.6	0.993	5.8	406	16	3.9
1056	1093	96.6	0.995	5.3	406	17	4.2
1206	1247	96.7	0.996	5.1	406	19	4.7
1356	1403	96.7	0.996	4.9	406	22	5.4
1506	1558	96.7	0.996	4.8	406	24	5.9
1660	1715	96.8	0.997	4.7	406	26	6.4
1810	1870	96.8	0.997	4.7	406	28	6.9
1958	2020	96.9	0.997	4.5	406	31	7.6
2108	2173	97.0	0.997	4.4	406	33	8.1
2254	2322	97.1	0.987	4.3	406	38	9.4
2407	2480	97.1	0.987	4.3	406	41	10.1
2559	2640	96.9	0.988	4.2	406	41	10.1
2792	2894.0	96.5	0.988	4.2	406	42	10.3
2981	3095.0	96.3	0.989	4.1	406	43	10.6

Table 3. Measurements for Vinac = 230 Vac

Pout	Pin	eff.(%)	PF	THD	Vout	Voutripple	Ripple%
156	163	95.7	0.870	25.4	406	8	2.0
306	317	96.5	0.964	15.2	406	12	3.0
456	471	96.8	0.978	11.6	406	14	3.4
607	626	97.0	0.985	9.8	406	16	3.9
757	780	97.1	0.989	8.8	406	16	3.9
907	933	97.2	0.991	7.8	406	18	4.4
1057	1086	97.3	0.992	7.5	406	18	4.4
1207	1240	97.3	0.993	7.1	406	20	4.9
1356	1395	97.2	0.994	6.8	406	22	5.4
1506	1550	97.2	0.995	6.6	406	24	5.9
1657	1706	97.1	0.995	6.4	406	28	6.9
1807	1863	97.0	0.996	6.2	406	29	7.1
1958	2020	96.9	0.996	5.9	406	31	7.6
2108	2178	96.8	0.996	5.8	406	33	8.1
2260	2340	96.6	0.996	5.8	406	35	8.6
2408	2493	96.6	0.996	5.6	406	38	9.4
2558	2650	96.5	0.997	5.6	406	40	9.9
2816	2920	96.4	0.998	5.5	406	42	10.3
2981	3091	96.4	0.998	5.4	406	43	10.6

Table 4. Measurements for Vinac = 265 Vac

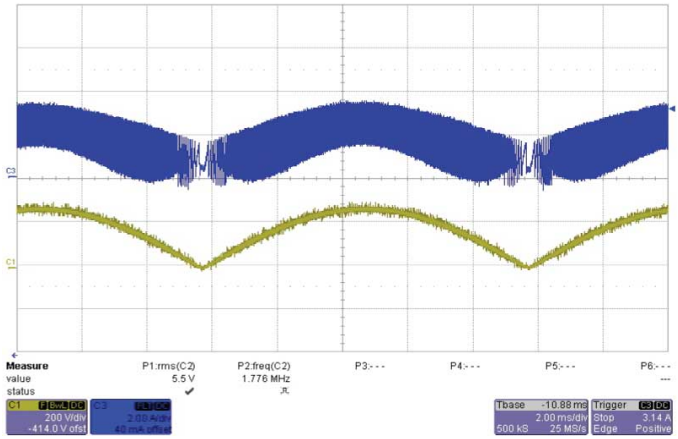
Pout	Pin	eff.(%)	PF	THD	Vout	Voutripple	Ripple%
156	163	95.7	0.830	30.0	406	8	2.0
307	318	96.5	0.950	15.7	406	12	3.0
457	470	97.2	0.970	15.7	406	15	3.7
606	623	97.3	0.975	15.4	406	16	3.9
757	777	97.4	0.978	15.4	406	19	4.7
906	930	97.4	0.981	15.3	406	21	5.2
1056	1084	97.4	0.983	15.0	406	21	5.2
1206	1237	97.5	0.983	15.1	406	22	5.4
1356	1391	97.5	0.984	15.1	406	23	5.7
1507	1546	97.5	0.985	15.1	406	26	6.4
1658	1702	97.4	0.985	15.1	406	28	6.9
1807	1858	97.3	0.986	14.9	406	30	7.4

Table 4. Measurements for Vinac = 265 Vac (continued)

Pout	Pin	eff.(%)	PF	THD	Vout	Voutripple	Ripple%
1959	2013	97.3	0.986	14.9	406	33	8.1
2110	2168	97.3	0.986	14.8	406	35	8.6
2257	2320	97.3	0.998	14.8	406	35	8.6
2408	2480	97.1	0.998	14.7	406	38	9.4
2562	2640	97.0	0.998	14.6	406	40	9.9
2822	2916	96.8	0.999	14.5	406	41	10.1
2987	3093	96.6	0.999	14.4	406	42	10.3

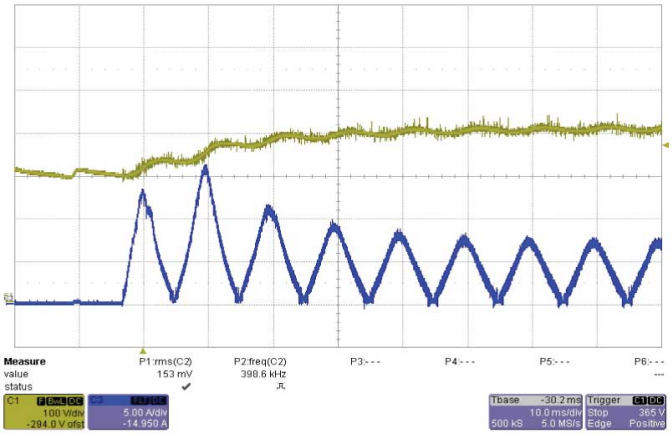
Figure 10 is an image showing the current on the boost inductor in blue and the input voltage in yellow. The working conditions are: Vinac=220 AC; Pout=500 w. As can be seen, at this power level the working mode is already continuous in almost all the semiperiod of the input AC.

Figure 10. Scope acquisition. Working conditions: Vinac=220 AC; Pout=500 W



In this second image (*Figure 11*) a simulation of startup, with a connected load, of 1200 W is shown.

Figure 11. Scope acquisition: startup with a connected load of 1200 W



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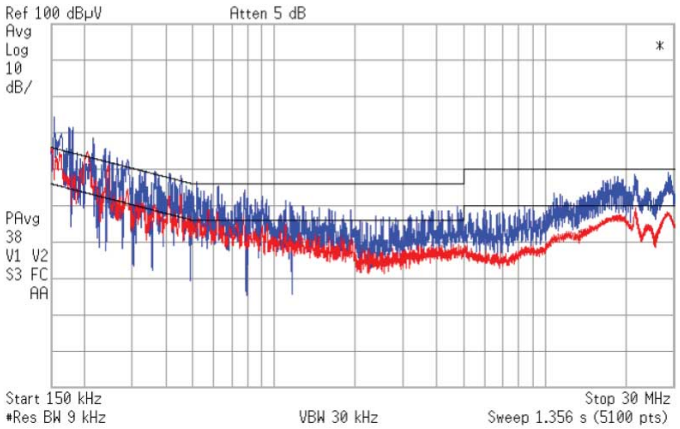
All the magnetic parts present on the board and designs for the input and output filter to make the system IEC55014 and IEC55022 compliant are provided by MAGNETICA.

Figure 12 is an image showing the conducted emission after the design and assembling of the filter.

Figure 12. EMI tests after the design and assembling of the filters



AM03639v1

9 Revision history

Table 5. Document revision history

Date	Revision	Changes
22-Jun-2010	1	Initial release.

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